REMARKS

Applicants appreciate the examination of the present application that is evidenced by the Official Action of December 13, 2004. Applicants also appreciate the indication that Claims 12-22 are allowed and Claims 6-11 recite allowable subject matter. In response to the Official Action, Claims 6, 7 and 11 have been rewritten in independent form to place Claims 6-11 in condition for allowance. In addition, minor grammatical amendments have been made to Claims 8-10, 12, 14-17 and 21 and Claims 23-24 have been canceled without prejudice.

Thus, the sole outstanding issues for consideration are the patentability of Claims 1-5 in view of U.S. Patent Nos. 6,392,462 to Ebuchi et al., the primary reference, and 6,794,912 to Hirata et al., the secondary reference.

Claim 1 is Patentable Over the Cited References

Applicants acknowledge that FIG. 11 of Ebuchi et al. discloses a multiphase clock generator that generates a plurality of output clock signals (shown as PH1-PH10). However, Ebuchi et al. does not disclose or suggest the subject matter of Claim 1 for at least two reasons. First, all the output clock signals PH1-PH10 in FIG. 11 of Ebuchi et al. have the same frequency, not "different frequencies" as required by Claim 1. Second, none of the clock signals PH1-PH10 having "full-period programmable skew characteristics," as required by Claim 1. As illustrated best by FIG. 23 of Ebuchi et al., none of the clock signals PH1M-PH10M, which are provided as inputs to the switching circuit **610** in FIG. 11, has a full-period programmable skew characteristic. For example, the skew of the first clock signal PH1M cannot be adjusted at all in response to the select signal PHSEL[0:3] (i.e., PH1M always has the same phase as PHA1) and the skew of the last clock signal PH10M can only be adjusted to have four different skews (shown by PHA10, PHA9, PHA7 and PHA3), which do not span a full period as required by Claim 1. Moreover, even if the clock signals PH1M-PH10M are routed through one of the illustrated frequency divider circuits **510**, **200**, **400** or **500**, all of the output clock

signals PH1-PH10 will retain the equivalent frequency and have less than full period skew control. Thus, notwithstanding the disclosure of Ebuchi et al., Applicants respectfully submit that Claim 1 is patentable over the cited prior art.

CONCLUSION

Applicants have addressed each of the outstanding issues raised in the first Official Action and have shown that Claim 1 is patentable over the cited prior art references. Applicants have also rewritten many of the allowable dependent claims into independent form to place them in condition for allowance. Accordingly, Applicants submit that the present application is in condition for allowance, which is respectfully requested. The Examiner is encouraged to contact the undersigned by telephone in the event any issues remain which may prevent issuance of the present application.

Respectfully submitted,

Grant J. Scott
Registration No. 36,925

USPTO Customer No. 20792
Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, North Carolina 27627
Telephone: 919/854-1400
Facsimile: 919/854-1401

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 16, 2004.

Candi L. Riggs

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